CM7104 Codec & CM6530N USB Audio

High Speed Audio DSP with Hi-Fi Audio Codec

Low Power for Headset / Microphone / Docking

Application Notes

ver.1.00
Sept 10, 2024

NOTICES

THIS DOCUMENT IS PROVIDED “AS IS” WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, DOCUMENT OR SAMPLE.

COPYRIGHT

TRADEMARKS

Cmedia, the Cmedia Logo, Xear 3D, Xear 3D Logo, Speaker Shifter, Smart Jack, and Smart Audio Jack, Middleware are trademarks of C-Media Electronics Inc. in Republic of China and/or other countries. All other brand and product names listed are trademarks or registered trademarks of their respective holders and are hereby recognized as such.

TABLE OF CONTENTS

Release Note

Revision	Date	Description
1.00	2024/9/10	First release

1 About This Document

The CM7104 is a highly-integrated Audio DSP plus CODEC system whose high-performance and low-power consumption make it ideal for a wide range of mobile systems, such as Tablet, Smartphone and Ultra-book. The CM7104 DSP core, Tensilica HiFi EP, with extensive memory resources provides low-power advanced digital signal processing. Given that Tensilica HiFi core is widely used by many third-party software developers, it makes CM7104 create an extensive wide software reference design ecosystem, including multi-microphone advanced voice processing (NS, AEC…etc.), low power speech trigger and recognition, and high-quality well-known branding audio post-processing. The CM7104 integrates a fully-flexible digital mixing and routing with asynchronous sample rate converter (ASRC) to support the DSP core for wide use case flexibility. Two digital audio interfaces are provided, supporting I2 S/PCM/TDM audio formats. Two differential analog microphone inputs and up to four digital microphone inputs can accept audio signals from multiple microphone or line input sources. Two differential line outputs can provide high performance analog audio signal outputs for connecting high-quality amplification systems. The CM7104 also combines a variety of low-power fixed-function signal processing components. The advanced multiband DRC (Dynamic Range Control) enables further digital audio processing capabilities on playback or record paths. Advanced DRC function comprises multi-section and multi-band parts, ensuring signal level maintenance, maximizes loudness, and prevents audio clipping and speaker damage. The CM7104 can be powered from a 1.8V power supply only, and its individual blocks are all design for power efficient target, helping devices to achieve long time playback, record, voice talk…etc. cases. The CM7104 is supplied by a LQFP48 package within 7x7 mm

The purpose of this document is to summarize the common application notes for customers who are designing their products with CmediaCM7104 & CM6530N USB audio processor series or who are evaluating the solutions. It will contain the following contents about the typical system block diagram; schematics design notes, layout guide, applicable PC OS & Apple IOS & Android, and exception notes. It's recommended to read this document before you start to plan and design your products with CM6530N USB audio solution.

2 Schematics Design Notes

2.1 Test Pin for firmware crash recover

Figure1. CM6530N Test Pin circuit.

When CM6530N firmware crashed, short Test Pin to 3.3V re-plug in PC could into Test Mode (Flash recover mode).

Notice!! CM6530N series default firmware is empty and have no function!! The device PID/VID always = 0D8C/0018.

When plug into pc will show

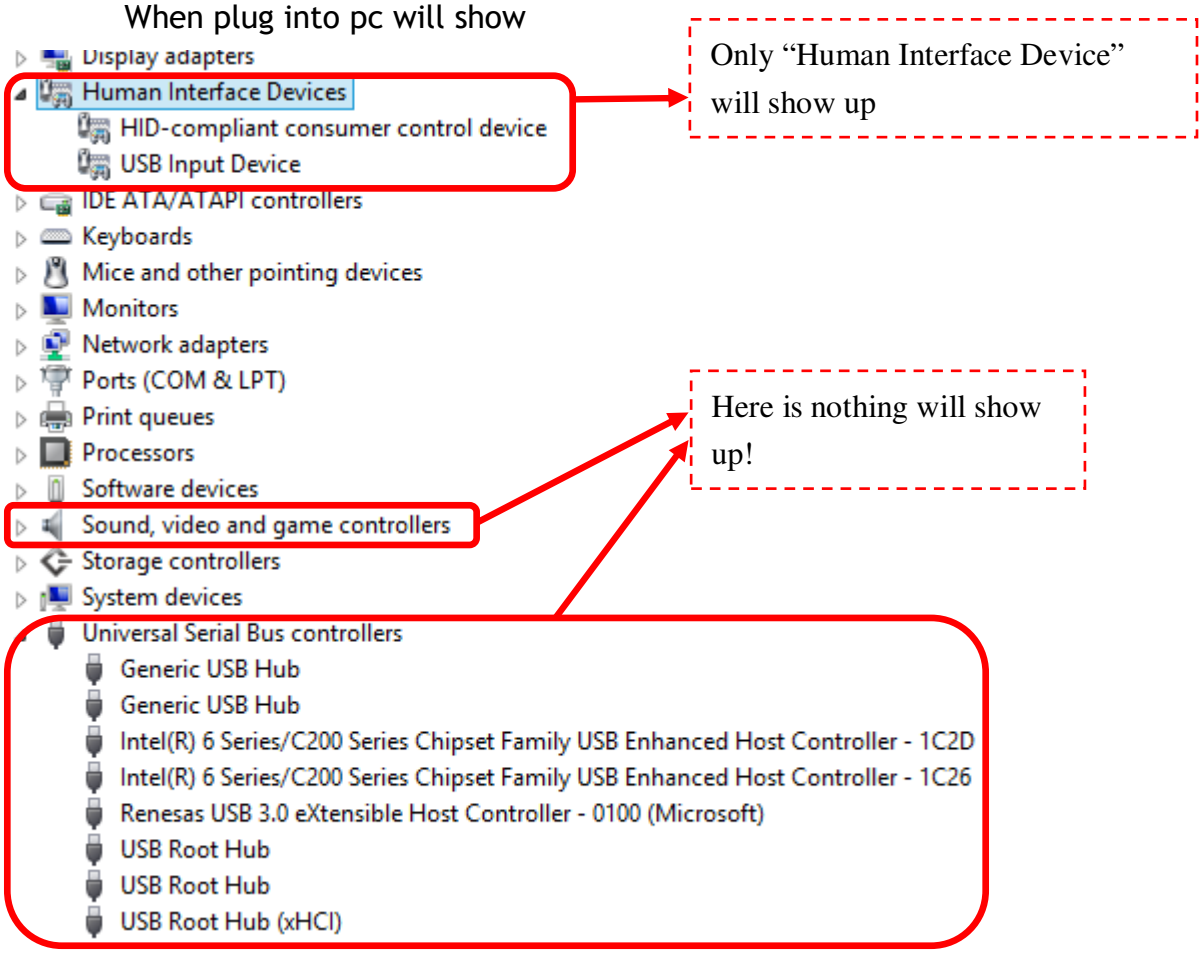


Figure1. CM6530N defaults only have HID function.

2.2 Power Control Design

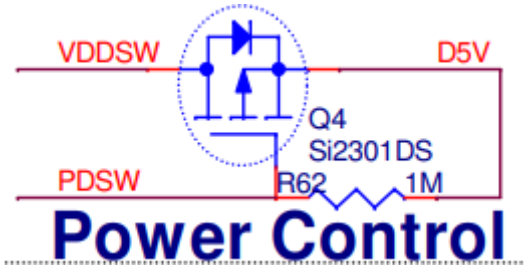


Figure2. CM6530N power control circuit.

OS Mode	PDSW	VDDSW1
Operation	Drive Low	5V
Suspend	Open	0V

2.3 Crystal Design

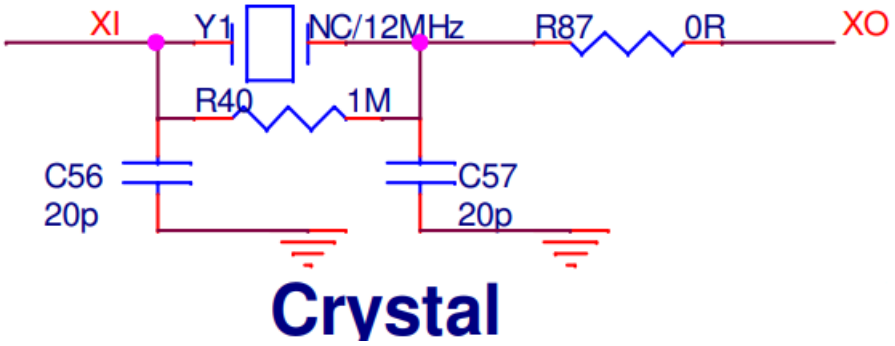


Figure3. CM6530N crystal circuit.

.

2.4 USB Interface & GND Separate Design

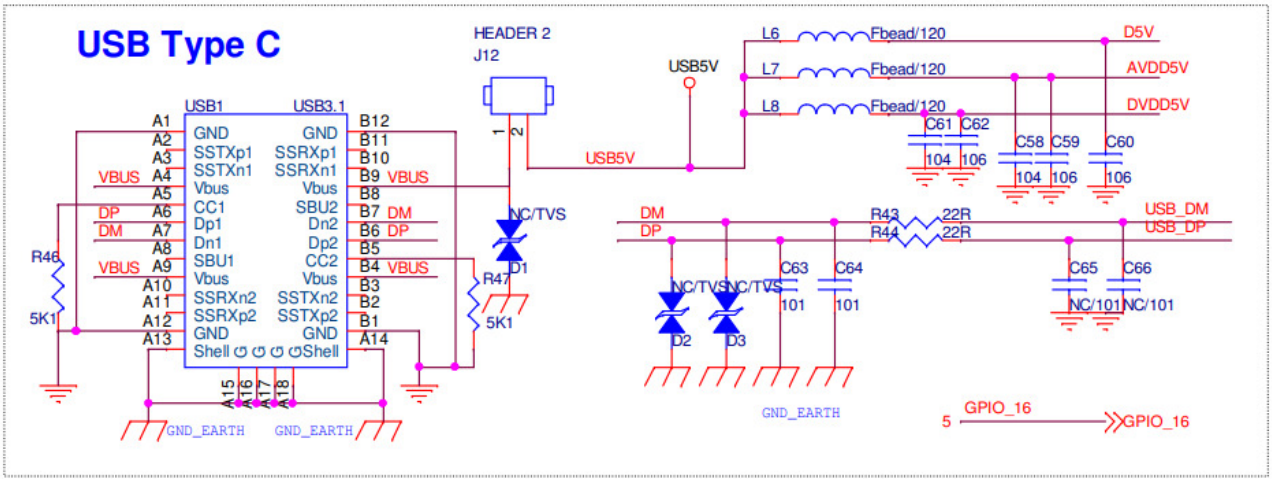


Figure4. CM6530N USB & GND separate circuit.

- R1 & R4 for USB PHY impedance matching.
- C1 & C2 for EMI solution.
- D2, for ESD solution.

Digital GND & Shielding GND separate by Fbead.

USB TVS(D1) Choose Suggest

Device Descriptions	Rising Time	Data Rate	Suggested capacitor
USB 1.1	4~20 nS	12 M bps	3~40pF

2.5 HID Button

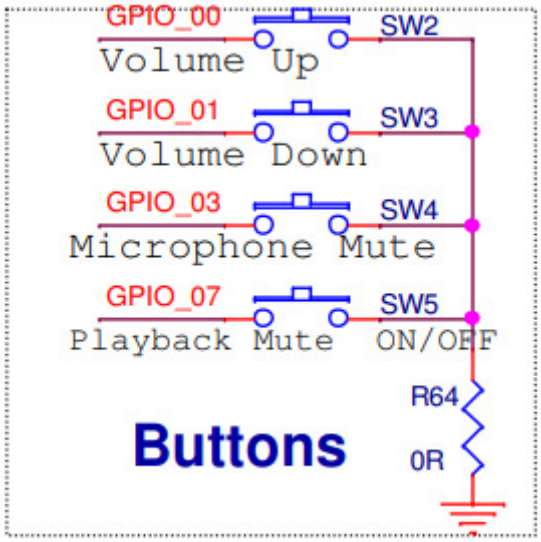


Figure5. CM6530N HID Button circuit.

CM6530N Support HID Button. Use CM6530N GPIO (default pull high), when push the button will drive low, and trigger firmware report function to OS.

Default support:

-Volume Up (GPIO_00)

-Volume Down (GPIO_01)

-Record Mute(GPIO_03)

-Playback Mute(GPIO_07)

3 Colors LED

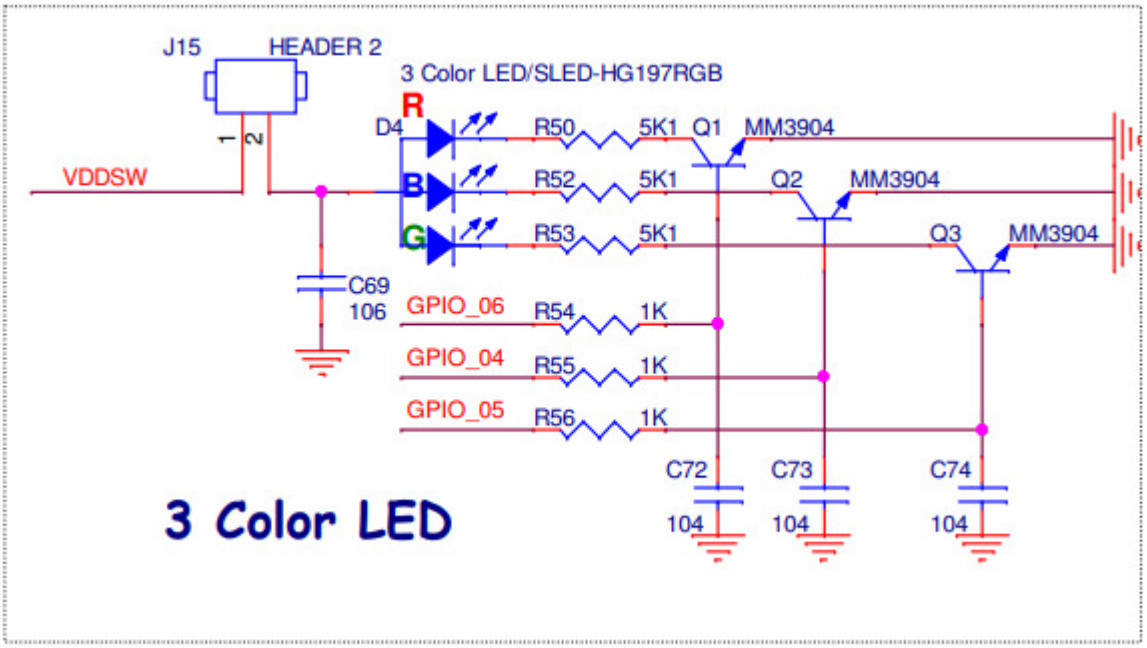


Figure6. CM6530N Common-anode high brightness 3 Color LED circuit.

Common-anode 3 Color high brightness LED (20mA each LED) control need a NPN transistor (Q1, Q2, Q3) provide higher power. And GPIO 04~06 is PWM signal, layout must follow layout guide.

CM6530N Support 3 colors (Red, Green, Blue) LED, need firmware program it.

2.6 DC to DC Power Design

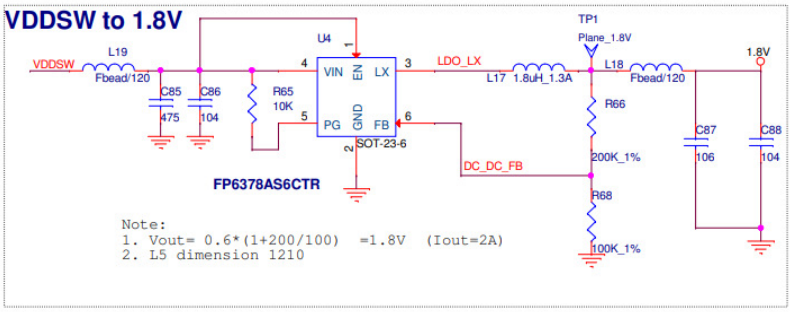
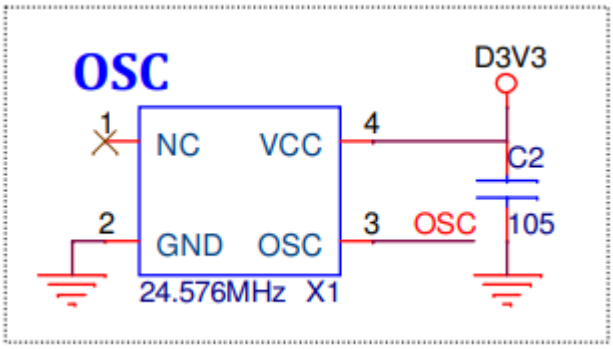


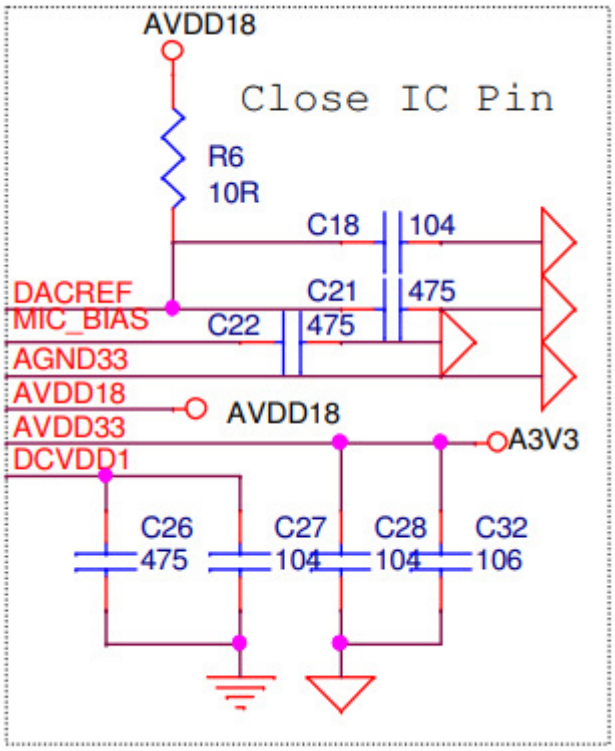
Figure7. CM6530N DC to DC power control circuit.

The DC to DC power had much switching noise, so the layout must be note. GND must connect to shielding DGND.

2.7 CM7104 Oscillator 24.576MHz



2.8 CM7104 bypass capacitor close IC pin



2.9 GPIO External Pull-Low Resistor

When GPIO is used for input, GPIO external pull-low resistor recommended to using lower than 100 Ω.

3 Layout Guide

This document provides guideline for the design of USB audio PCB. It's important to ensure maximum performance proper component placement and routing. This document includes properly isolated digital circuitry and analog circuitry. The effects of ground loop and supply plane geometry, decoupling/ bypassing/ filtering capacitors placement priorities, USB D+ and D- signals, analog power supplies, and analog ground planes.

3.1 General Rules

1. If it's necessary to turn 90°, it's better to use two 135° turn (keep angles >= 135°) or an arc, instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

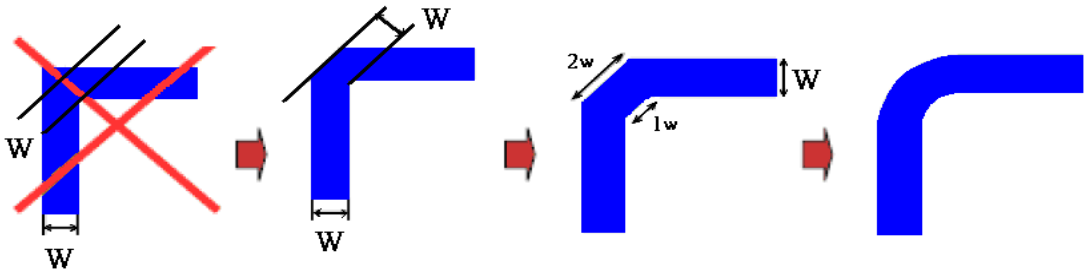


Figure11. Turn angle.

Figure11. Turn Angle

2. The old rules of splitting power and ground into "digital" and "analog" sections do necessarily apply to the many audio devices. AGND and APWR plane as the same region as possible, place DGND and DPWR plane on other region.
3. Use Ferrite Bead to connect different ground plane to avoid the EMI issue.

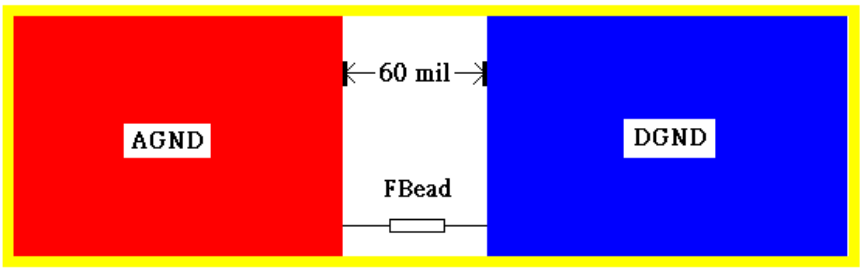


Figure12. AGND & DGND.

4. Connect analog and digital power planes at one point through a low impedance

bridge or preferably through a ferrite bead.

5. To achieve proper ESD/EMI performance; it's suggested to use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the connector pin. If voltage regulators are used, place a 0.1μF capacitor on both input and output. This is to increase the immunity to ESD and reduce EMI.

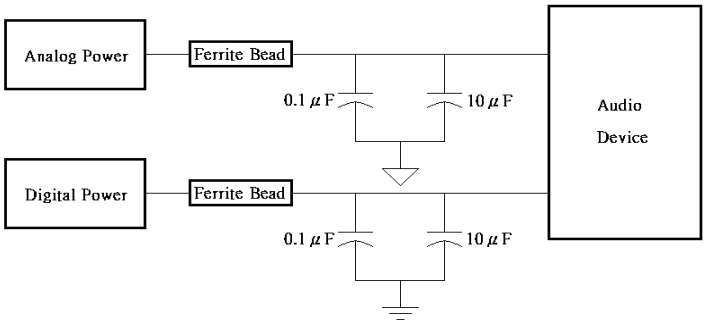


Figure13. Capacitors array.

6. Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

3.2 Differential Signal Pair Impedance Matching

The USB D+ D- differential pairs, which can operate at a rate of 12Mbit/s, are some of the most critical signals on a PCB. Its implementation on the PCB requires special considerations. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as detail below.

Differential: Impedance of 90Ω, is optimal

Single-end: Impedance of 45Ω, is optimal

1. Place CM6531N USB Audio Controller chip as close as to the USB connector and place it on the un-routed board first, with minimum trace lengths, as equal as possible, route full-speed differential signal pair first. Keep appropriate distance between full-speed signals to USB differential signal pair.

2. Route the USB differential signal pair on the component side, which is adjacent to the ground plane layer. Vias to different signal trace layers or routing to close to breaks in the ground plane will adversely affect the differential trace impedance.

3. Route USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change.

4. Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference.

5. Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality.

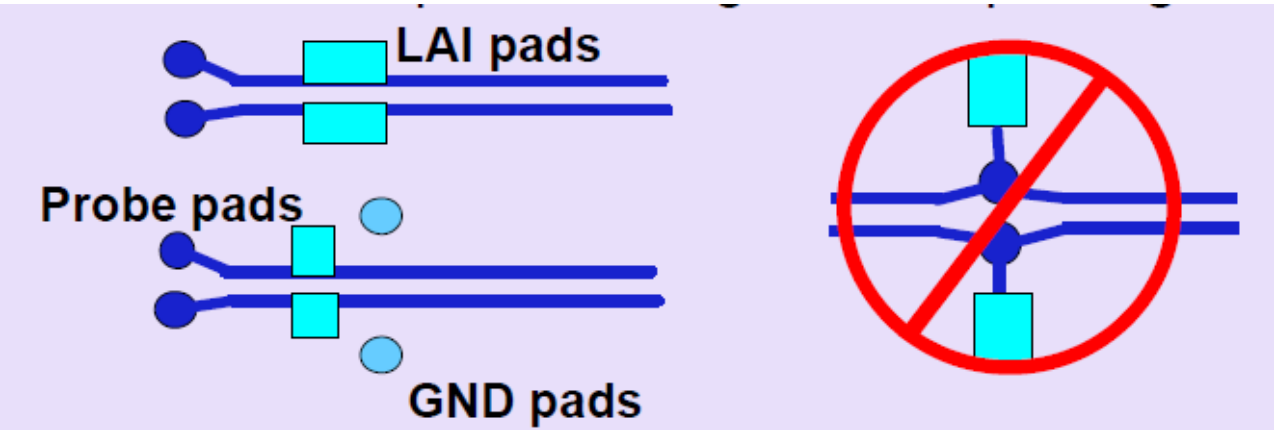


Figure14. Stubs affect.

6. Route USB differential signal pair traces over continuous ground and power planes. Avoid differential signal pair crossing anti-etch areas or any break in the underlying planes and routing the near the edge of the PCB or power planes.

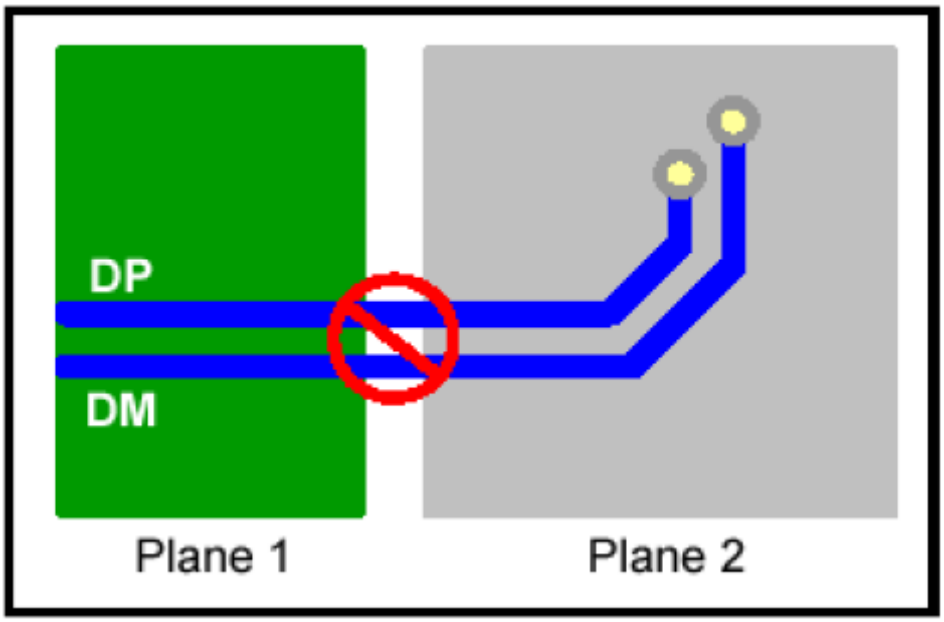


Figure15. Route USB traces fail.

7. Keep parallelism between PERp0/PERn0; PETp0/PETn0 and REFCLK+/REFCLK- with the same trace spacing, which achieves 100Ω differential impedance.

8. Route paths of SPDIF IN and OUT to separate t least 20 mils gap.

9. Do not allow any digital or analog signal traces pass through the drawbridge, otherwise, the digital noise may induced into the analog signals, makes audio performance worse.

10. Avoid crossing the image power or ground plane boundaries with full-speed clock signal traces immediately above or below the separated planes. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through screw holes.

11. Cmedia recommended to layout the width of each signal traces at least 10 mils and the space is the least one time the size of width of signal trace.

12. For ADC and DAC, VREF is also bypassed. Depending upon the converter architecture, the range of the large capacitor may be from 1uF to 47uF. Place bypass capacitor near chip.

13. Placement of the capacitor near the chips is very important. The bypass capacitors provide full speed current for the modulator operation, so the bypass capacitors are actually used to store charge for this full speed current draw.

3.3 Layout design of Ground and Supply Plane geometry

The layout separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from clean analog audio circuitry. The digital and analog ground planes are tied together by a wide link (about 50mils) at a point close to the USB connector. This will be the "drawbridge" that goes across the moat. Do not allow any digital or analog signal traces pass through the drawbridge. Otherwise, the digital noise may get into the analog signals and make audio performance worse.

In order to achieve the best audio performance and prevent crosstalk issue, Cmedia recommend that the width of each I/O signal trace be at least 10 mils and the space be at least one time the size of the width of signal trace.

For a layout that helps to reduce noise, separating analog and digital ground planes is needed. The digital components should be placed over the digital ground plane, and the analog components (including the analog power regulators) should be placed over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their ground planes. Place analog power coincident with analog ground and digital power coincident with digital ground. If any portion of analog and digital plane overlaps, the distributed capacitance between the

overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolating the power planes. The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

3.4 Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise to ground. Commonly, USB audio controller may generate noise when its internal digital circuitry is operating. The current changes arise in the power and ground pins for the related section of the USB audio controller. The goal is to force AC current to flow in the shortest loop from the supply pin through the bypass cap and back into the USB audio controller through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the USB audio controller and the bypass capacitors when in the operating frequency of the USB audio controller. The long-trace will greater the inductance. To avoid long-trace inductance effects, use the shortest traces for bypass capacitors, with wide traces to reduce impedance. For the best performance, use supply bypass leads of less than one-half inch.

The USB audio controller power supply pins are need the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10μF surface mount devices are good if they are used in conjunction with 0.1μF ceramics. The filter capacitors with “B” priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to USB audio controller. A good reference voltage is relative to good analog performance. These decoupling capacitors should be close to the USB audio controller pins (Audio input pin), or positioned for the shortest connections to pins, with wide traces to reduce impedance.

3.5 The USB connector

Place the USB device and connector on the un-routed board first. With minimum trace lengths, as equal as possible (D+, D-), route full-speed clock and USB differential signal pair first. Keep the distance between full-speed signals to USB differential signal pair far. Route the USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change. If it’s necessary to turn 90°, it’s better to use two 45° turn or an arc instead of making a single 90° turn. It can reduce reflection

on the signal by minimizing impedance discontinuities.

Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference. Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and lower the quality. If a stub is unavoidable in the design, no stub should be bigger than 200mils.

3.6 Guard ring on PCB-edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 10 the field lines of the signal return to PCB ground as long as an "infinite" ground is available. Traces near the PCB-edges do not have this "infinite" ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable – should be accompanied by a guard ring on the PCB edge.

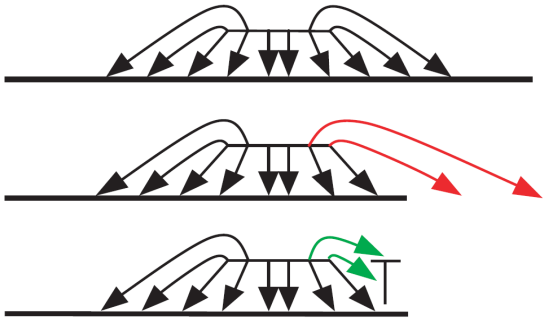


Figure16. The field lines of signal return to PCB ground.

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 10. As these traces should have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Advantages of power planes

1. Easy and fast to implement
2. Low inductive power supply
3. Creates a capacity together with ground plane

Advantages of routed power supplies

1. Allows the usage of one layer for more than one supply system, thereby reducing the cross -talk between these supplies
2. May reduce cross-talk within each supply system
3. Requires more careful power routing
4. Higher supply impedance may require extra capacity for supply stabilization.

The optimum obviously is to apply the advantages of both methods. Therefore several local power planes should be implemented and connected to the supply via traces. Planes of different supply systems should be located in the same layer or separated by a ground plane to minimize crosstalk between these systems. Although the local power planes are easy to implement special care must be taken when connecting the power pins and the decoupling capacities to the planes.

(a) Connection of decoupling capacities

The decoupling of the most critical power supply pins of the microcontroller (for identification of these refer to chapter 3) very often is the most fastidious part in a PCB design. Even in a multilayer design every millimeter of trace has to be carefully considered.

(b) Sketch equivalent circuits

When considering the best placement, direction and connection of the capacity a small sketch may be very useful. Each piece of wire shall be drawn as impedance even though the actual value is not important. The Figure 11 clearly indicates that the 2 red impedances should be minimized while the other 2 may be object to concessions.

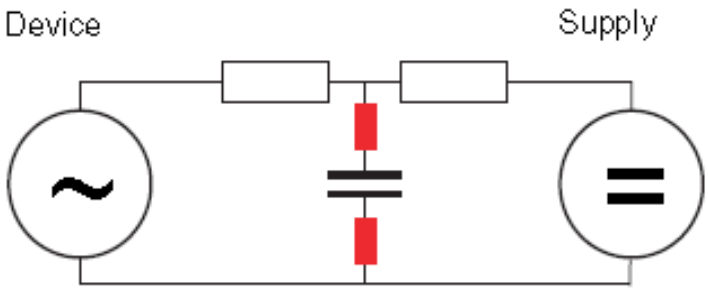


Figure17. Sketch equivalent circuit.

3.7 Cross Talk

A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 parts of next Figure indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.

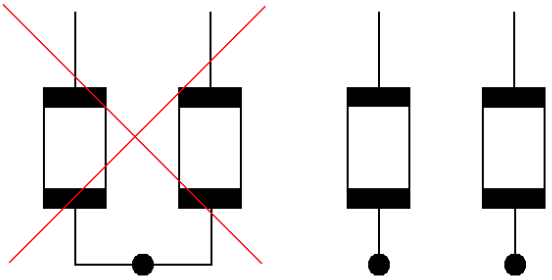


Figure18. Bad screw hole to Cross-Talk.

3.8 Return Current and Loop Areas

Image Planes

Return path or image planes provide low impedance, shortest possible path for return signal currents. The best image plane is the ground plane for the Cmedia USB Audio board.

Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

Avoid crossing the image power or ground plane boundaries with full-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane.

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source – the return current. With DC, the return current takes the way back with the lowest resistance. With a higher

frequency, the return current flows along the lowest impedance. This is directly beside the signal.

If this return path, mostly the ground plane, has a slot, the return current has to take another way and the results in a loop area. The larger the area, the more radiation and EMI problems occur. The designer has to make sure that the return current can flow directly underneath the signal trace. Another is to route the signal the same way as the return current flows.

3.9 ESD Protection System Design Consideration

ESD protection system design consideration is covered of the CM6531N's PCB.
. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy

— End of Data —

C-MEDIA ELECTRONICS INC.

6F., 100, Sec. 4, Civil Boulevard, Taipei, Taiwan 106 R.O.C.

TEL：886-2-8773-1100

FAX：886-2-8773-2211

E-MAIL：sales@cmedia.com.tw